INTEGRATED CIRCUIT HAVING A MEMORY CELL ARRAY CAPABLE OF SIMULTANEOUSLY PERFORMING A DATA READ OPERATION AND A DATA WRITE OPERATION

ABSTRACT OF THE DISCLOSURE

An integrated circuit comprising a memory cell array capable of simultaneously performing data read and write operations is provided. The integrated circuit to which inputs and outputs (IOs) are separately provided and to which a write address and a read address are simultaneously input during one period of a clock signal comprises a plurality of memory blocks, the memory blocks comprising a plurality of sub-memory blocks, a plurality of data memory blocks corresponding to the memory blocks, and a tag memory controlling unit, which writes data to the memory blocks or reads data from the memory blocks in response to the write address or the read address, wherein access to the same sub-memory block is not simultaneously performed when the write address and the read address are the same.